Chipset Overview

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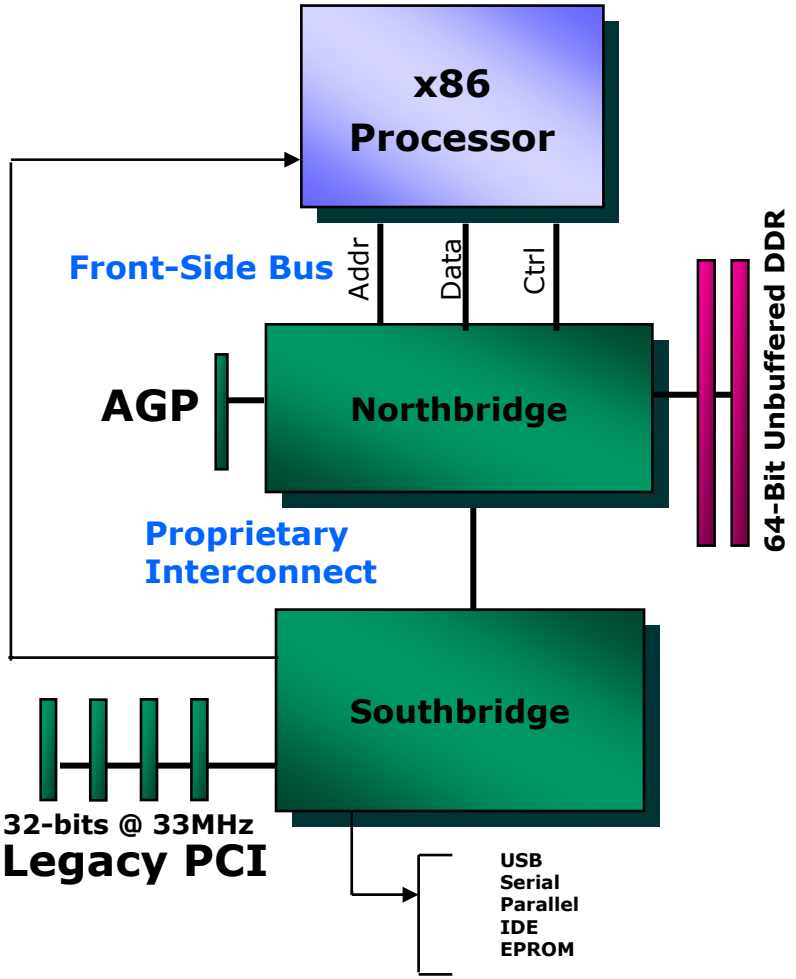
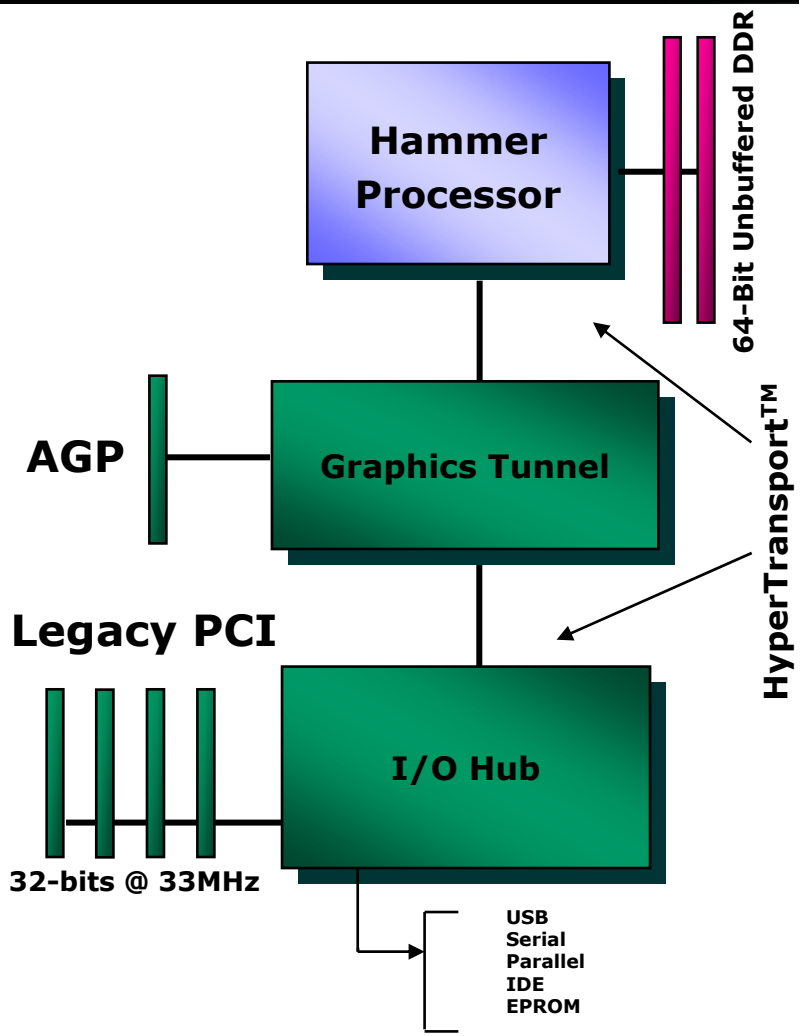
Current Generation Chipset

- Main memory supported by the chipset's Northbridge
  - Yields high latency CPU memory reads due to front-side bus, limiting CPU performance
- Multi-processor designs require different, more complex chipset
- Chipset design requires support of multiple busses
  - Front-side bus between processor and Northbridge
  - Proprietary bus between Northbridge and Southbridge
- Requires messy sideband signaling for power management



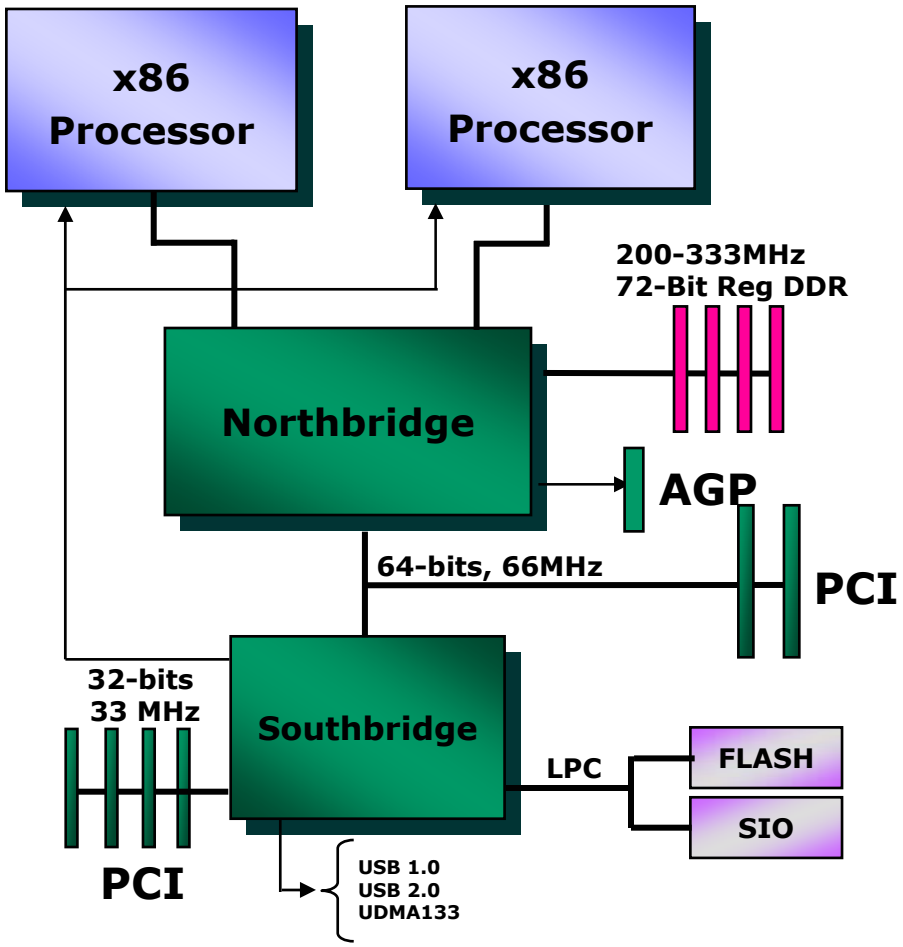
Hammer Chipset Value

- Integrated memory controller improves CPU performance and simplifies chipset design
  - Latency is very important to CPU performance: Hammer's integrated memory controller is designed to yield low latency
  - Bandwidth is important to I/O: HyperTransport™ provides high-bandwidth link between I/O and main memory
  - HyperTransport™ and Hammer CPU provide hooks for latency-critical I/O, such as graphics display refresh
- HyperTransport™ link creates glueless, scaleable architecture and simplifies chipset design
  - No proprietary inter-chip busses
  - HyperTransport™ is scaleable in link width and frequency

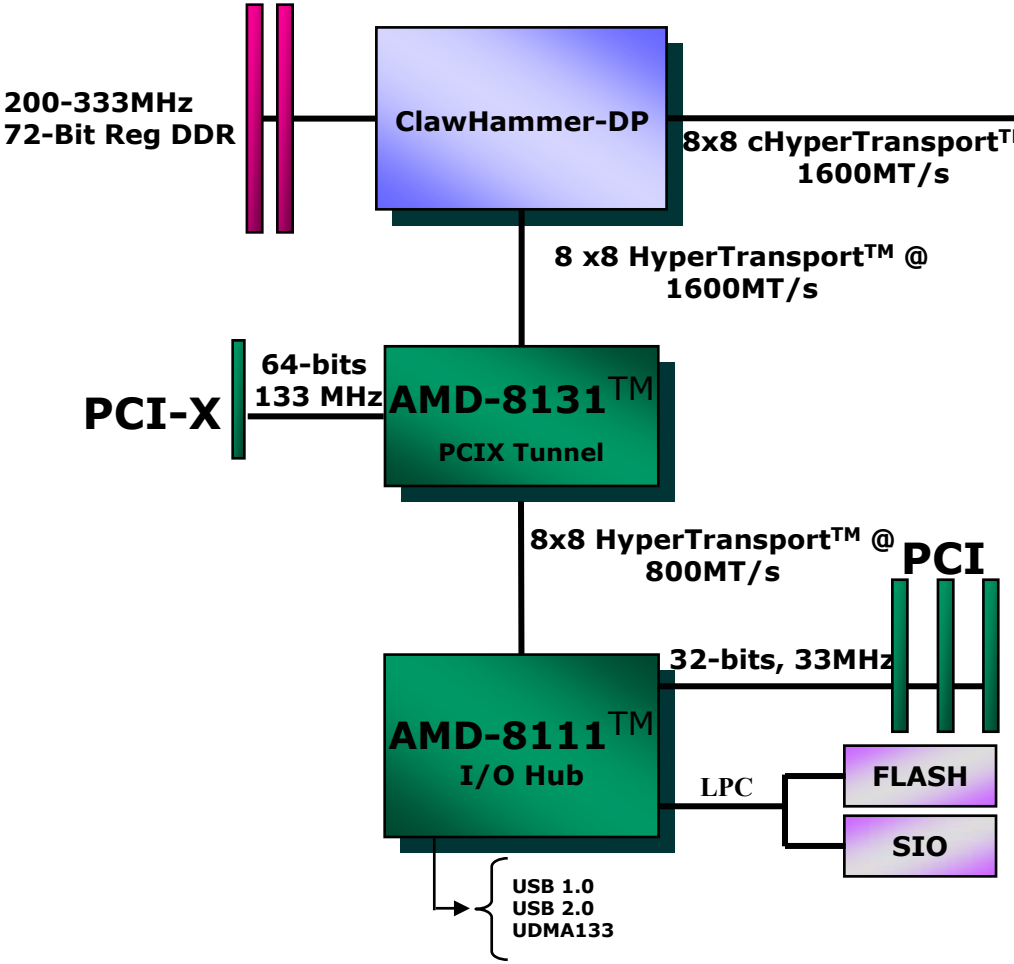


Current MP Architecture

- Northbridge memory controller provides limited total memory bandwidth to system
  - Memory bandwidth not scaleable with addition of second processor
  - High-latency due to front-side bus
- Requires special chipset for MP support
- I/O bus has limited bandwidth to main memory



Hammer MP Server Architecture

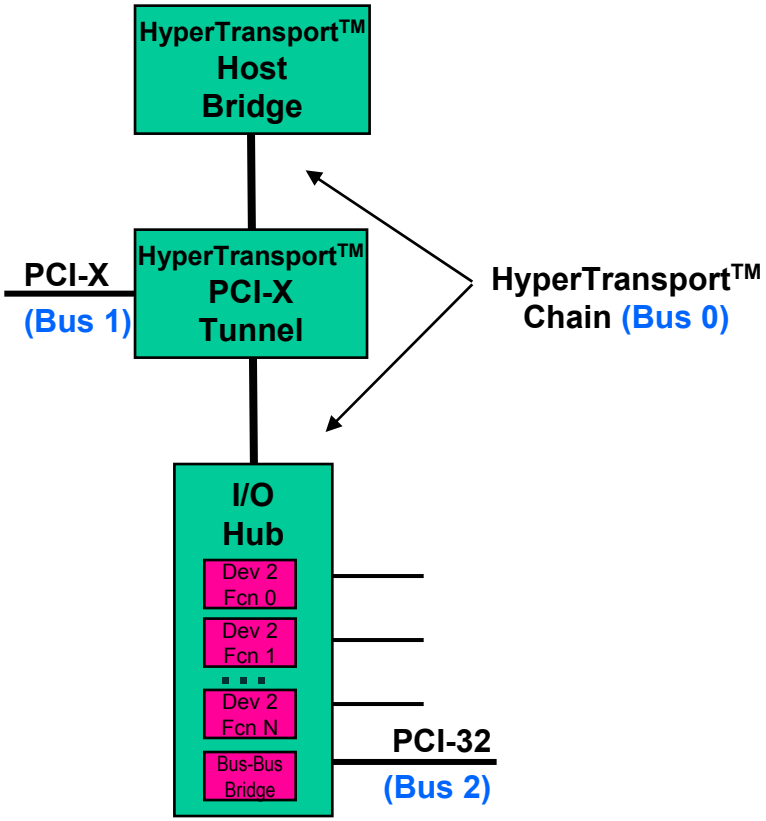


Scaleable architecture, allows increase of main memory bandwidth when adding second CPU

No additional chipset requirements for MP

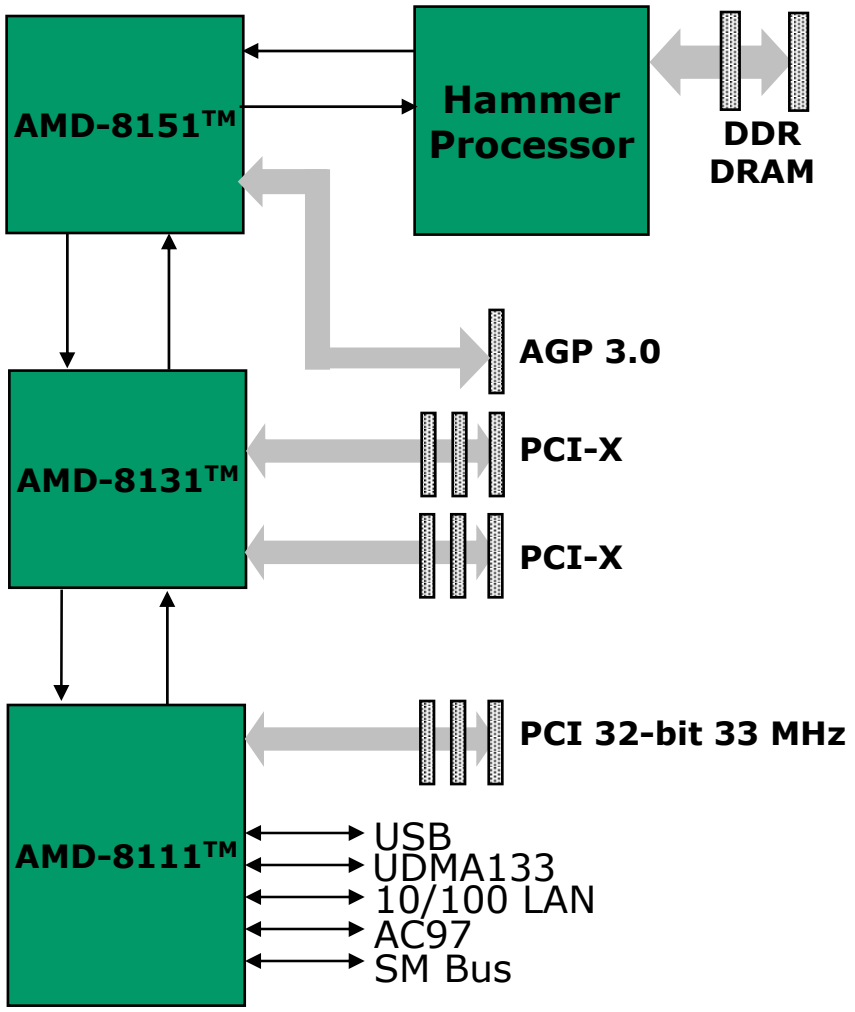
HyperTransport™ Tunnel

- HyperTransport™ tunnel architecture enables compatibility with PCI software infrastructure
  - Transparent to applications and operating systems
- Bus 0 transactions on primary bus destined for the I/O Hub are routed through the tunnel downstream to I/O Hub
  - Bus number does not change as it would in the case of a bridge
- Low latency through tunnels
- Hammer chipsets are based on this HyperTransport™ tunnel concept



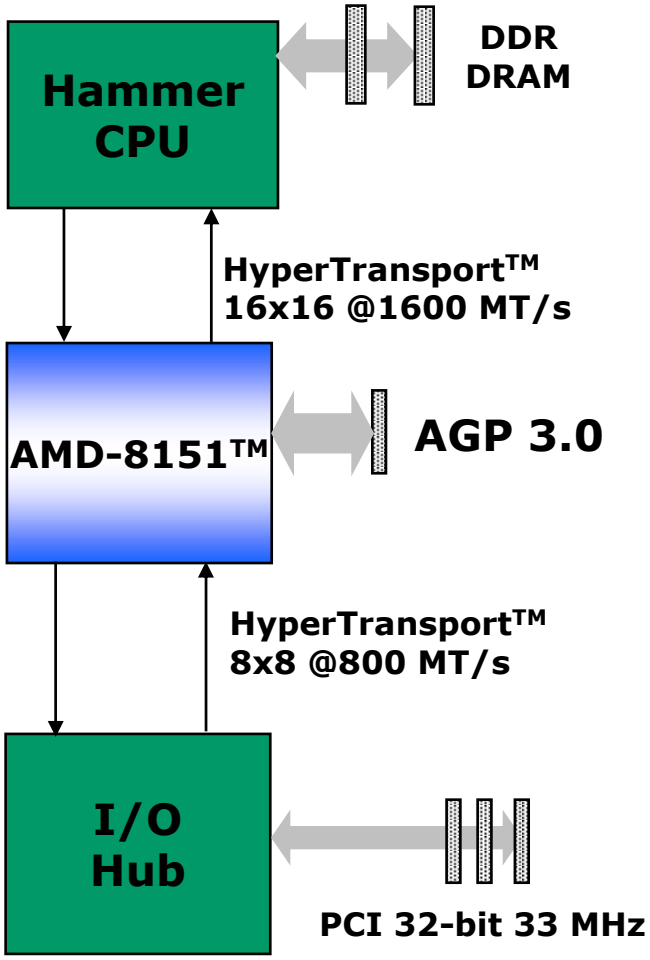
AMD Hammer Chipsets

- AMD chipset family provides the functionality required for typical desktop, mobile, and server platforms
- AMD-8151™ HyperTransport™ AGP 3.0 Tunnel for desktop, mobile and workstations
- AMD-8131™ HyperTransport™ PCI-X Tunnel for server and workstation platforms
- AMD-8111™ HyperTransport™ I/O Hub



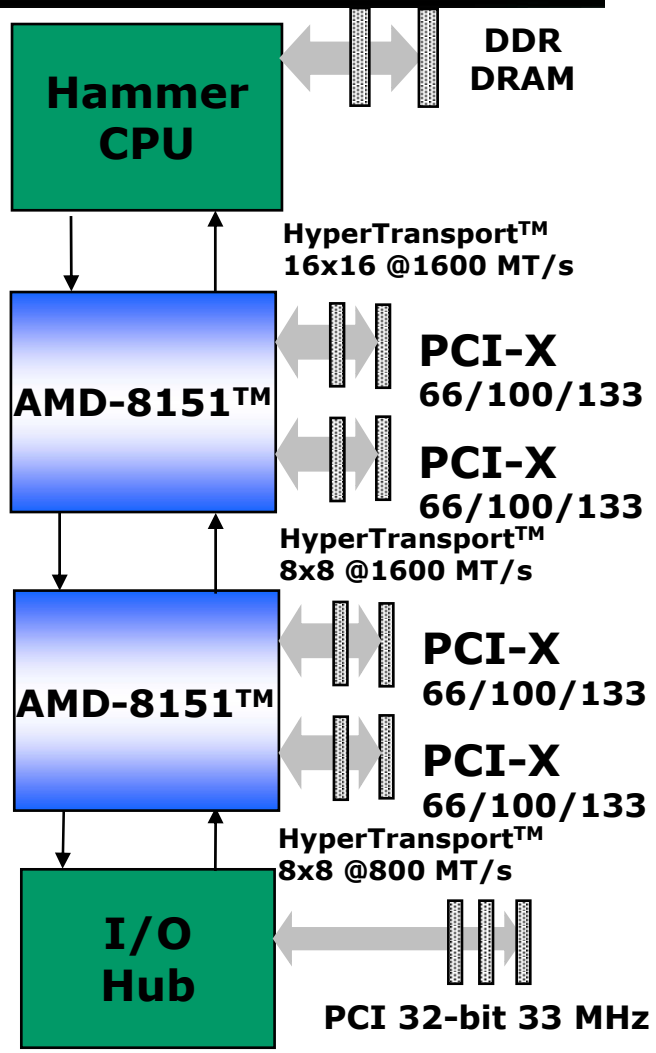
AMD-8151™ AGP Tunnel

- Two HyperTransport™ links
  - 16-bits side A, 8-bits side B
  - Side A supports up to 1600 MT/s, 6.4 GB/s max bandwidth
  - Side B supports up to 1600 MT/s, 3.2 GB/s max bandwidth
- AGP-8X bridge
  - AGP 3.0 specification signaling compliance, supporting 4X and 8X transfer rates
  - AGP 2.0 specification compliance for 1.5V signaling supporting 1X, 2X, and 4X transfer rates
- 31mm² package, 564 BGA package



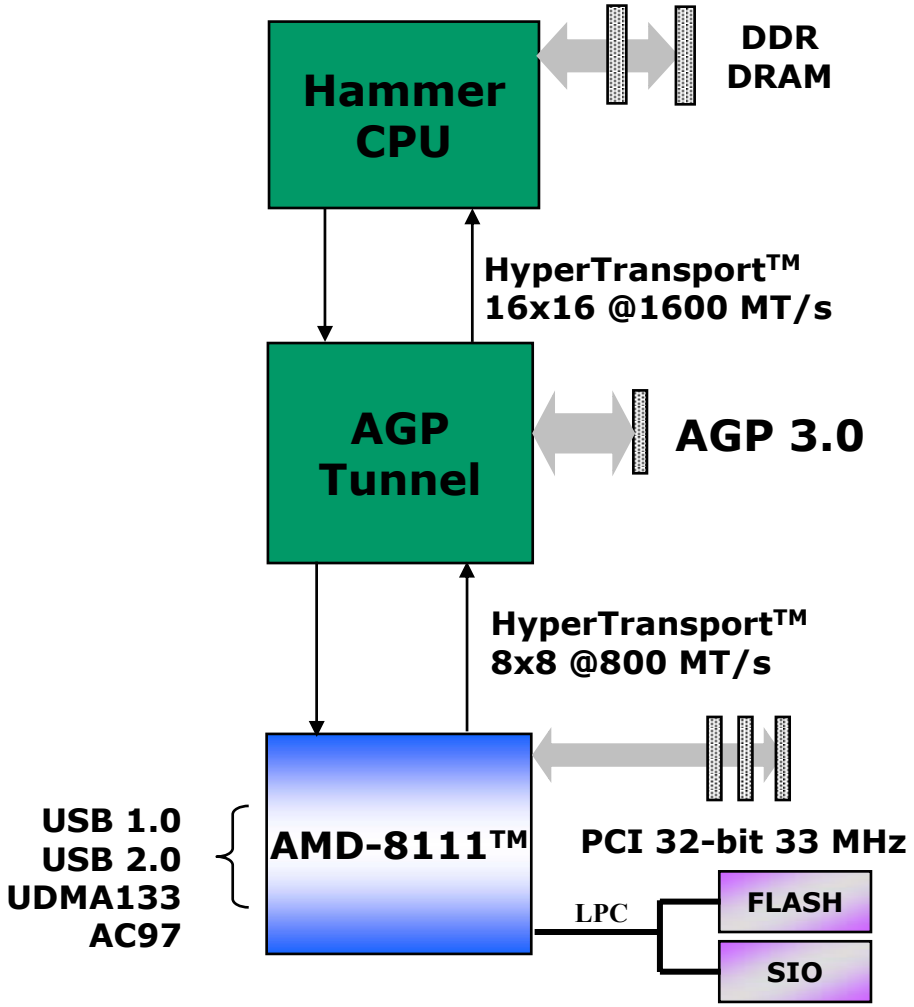
AMD-8131™ PCI-X Tunnel

- Two HyperTransport™ links
  - 16-bits side A, 8-bits side B
  - Each side supports up to 1600 MT/s
  - 6.4 GB/s max bandwidth side A
  - 3.2 GB/s max bandwidth side B
- Two identical PCI-X bridges
  - 64-bit data bus
  - Legacy PCI and PCI-X operation
  - PCI-X 66, 100, 133 MHz speeds
  - Legacy PCI 33 or 66 MHz speeds
  - Support up to 5 bus masters
  - SHPC Compliant hot plug controller
- 37.5 mm^2, 829-pin BGA package



AMD-8111™ I/O Hub

- 8-bit HyperTransport™ link
  - Supports up to 800 MT/s
  - 1.6 GB/s max bandwidth
- Legacy Southbridge functions including timers, DMA, PIC, etc.
- 32-bit, 33 MHz legacy PCI Bus
- 10/100 Ethernet LAN Controller
- AC97, version 2.2 compatible
- LPC Bus, SM-Bus
- USB 1.0 and 2.0 support
- Enhanced IDE, UDMA133
- 35 mm² 492-pin BGA package

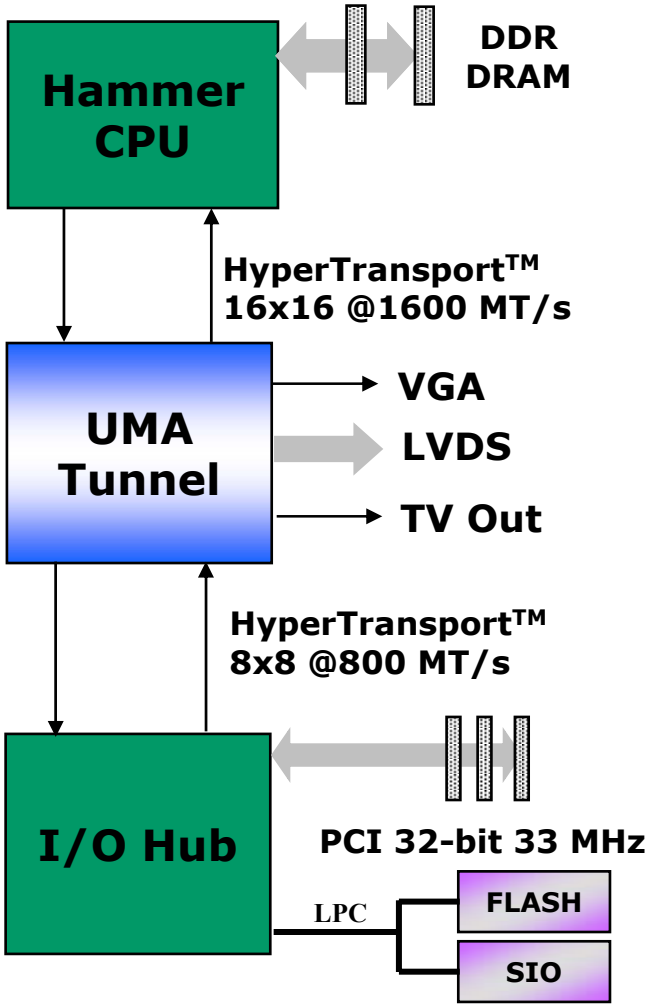


Chipset Power Management

- Chipsets control various power management features
  - ACPI C1, C2, C3, S1, S3 power management states
  - Thermal throttling
  - AMD PowerNow!™ technology frequency and voltage transitions
- Various levels of power management activities and power savings can be achieved based on system activity
  - Disconnect of HyperTransport™ links
  - Ramping of CPU core, Northbridge, and chipset clock domains
  - Placing main system memory in self-refresh
  - Dynamically lowering core frequency and voltage
- HyperTransport™ simplifies power management through the use of message-based protocol instead of sideband signals

Integrated Graphics Tunnel

- Integrated graphics for Unified Memory Architecture (UMA) yields significantly lower system cost than discrete graphics
- UMA requires high bandwidth and deterministic maximum latency for display refresh
  - HyperTransport™ protocol and Hammer Northbridge architecture provide both
- Several third-party chipset developers have announced plans to provide integrated graphics chipsets for Hammer platforms



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